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Date 1/14/03 Serial # 09/998594 Priority Application Date 08/857,100
Your Name Daniel St. Ger Examiner # 207 74513
AU 2876 Phone 305-2658 Room 6D07 (CP4)
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Other: _____

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What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Litigation Search of 09/998,594

Which is a continuation of 08/857,100

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Date Completed: _____
Searcher Prep/Rev Time: _____
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Terms: **patno=5984190** ([Edit Search](#))

857100 (08) 5984190 November 16, 1999

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5984190

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November 16, 1999

Method and apparatus for identifying integrated circuits

REISSUE: November 16, 2001 - Reissue Application filed Ex. Gp.: 2876; Re. S.N. 09/998,594 (O.G. May 28, 2002)

INVENTOR: Nevill, Leland R., Boise, ID

CERT-CORRECTION: February 19, 2002 - (O.G. March 12, 2002) a Certificate of Correction was issued for this patent

APPL-NO: 857100 (08)

FILED-DATE: May 15, 1997

GRANTED-DATE: November 16, 1999

ASSIGNEE-AT-ISSUE: Micron Technology, Inc., Boise, ID

ASSIGNEE-AFTER-ISSUE: May 15, 1997 - ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS)., MICRON TECHNOLOGY, INC. P.O. BOX 6 8000 S. FEDERAL WAY BOISE IDAHO 83707, Reel and Frame Number: 008567/0039

LEGAL-REP: Seed and Berry LLP

PUB-TYPE: November 16, 1999 - Utility Patent having no previously published pre-grant publication (A)

PUB-COUNTRY: United States (US)

US-MAIN-CL: 235#492

US-ADDL-CL: 235#494, 438#10, 438#18

CL: 235, 438

SEARCH-FLD: 235#492, 235#493, 235#494, 235#487, 438#10, 438#18

IPC-MAIN-CL: G 06K019#6

PRIM-EXMR: Hajec, Donald

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1/16/03

US 5,984,190

09/998594

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Selected file: PLUSPAT /

Search statement 2

?us5984190/pn

** SS 2: Results 1

Search statement 3

?prt fu legalall max

1/1 PLUSPAT - (C) QUESTEL-ORBIT

PN - US5984190 A 19991116 [US5984190]

TI - (A) Method and apparatus for identifying integrated circuits

PA - (A) MICRON TECHNOLOGY INC (US)

IN - (A) NEVILL LELAND R (US)

AP - US85710097 19970515 [1997US-0857100]

PR - US85710097 19970515 [1997US-0857100]

IC - (A) G06K-019/06

EC - H01L-023/544

PCL - ORIGINAL (O) : 235492000; CROSS-REFERENCE (X) : 235494000 438010000
438018000

DT - Corresponding document

CT - US4967381; US5103166; US5226118; US5294812; US5301143; US5313174;
US5380998; US5389770; US5420796; US5434870; US5467304; US5511005;
US5787174; EP0488053 A1; EP0578410 A2; DE3138085 A1; DE3226733 A1;
GB2244339

STG - (A) United States patent

AB - An integrated circuit and method for identifying same is described. The integrated circuit includes a programmable identification circuit for storing electronic identification information. The integrated circuit also includes an optical identification mark displaying a machine-readable optical identification code which corresponds with the electronic identification information stored in the identification circuit. The data encoded in the optical identification code may be identical with that of the electronic identification information. Alternatively, a look-up table or other correlating means may be employed to associate the optical identification code with the electronic identification information. The integrated circuit is packaged in a housing, and another optical identification mark is placed on an external surface of the housing. This second optical identification mark displays a machine-readable optical identification code which is identical or correlated to the electronic identification information stored in the identification circuit and/or the optical identification code displayed by the optical identification mark on the integrated circuit. Consequently, convenient and traceable identification of individual integrated circuits is provided during and after manufacture.

1/1 LGST - (C) LEGSTAT

PN - US 5984190 [US5984190]

AP - US 857100/97 19970515 [1997US-0857100]

DT - US-P

ACT - 19970515 US/AE-A

APPLICATION DATA (PATENT)

1/16/03

US 5,984,190

09/998594

{US 857100/97 19970515 [1997US-0857100]}

- 19991116 US/A
- PATENT
- 20020219 US/CC
- CERTIFICATE OF CORRECTION
- 20020528 US/RF
- REISSUE APPLICATION FILED
- 20011116
- UP - 2002-24

1/1 CRXX - (C) CLAIMS/RRX

AN - 3235485

PN - 5,984,190 A 19991116 [US5984190]

PA - Micron Technology Inc

PT - M (Mechanical)

ACT - 20011116 REISSUE REQUESTED

ISSUE DATE OF O.G.: 20020528

REISSUE REQUEST NUMBER: 09/998594

EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2876

Reissue Patent Number:

UP - 2002-11

UACT- 2002-05-28

1/2 PAST - (C) Thomson Derwent

AN - 200222-001900

PN - 5984190 A [US5984190]

DT - A (UTILITY)

OG - 2002-05-28

CO - REA

ACT - REISSUE APPLICATION FILED

SH - REISSUE APPLICATION FILED

2/2 PAST - (C) Thomson Derwent

AN - 200211-000245

PN - 5984190 A [US5984190]

DT - A (UTILITY)

OG - 2002-03-12

CO - COR

ACT - CERTIFICATE OF CORRECTION

SH - CERTIFICATE OF CORRECTION

Search statement 3

?file inpadoc

Selected file: INPADOC

Search statement 2

?fam us5984190/pn

1 Patent Groups

Stic EIC 2800

Darcy Bates

306-5419

1/16/03

US 5,984,190

09/998594

** SS 2: Results 6

Search statement 3

?famstate nonstop

1/6 INPADOC - (C) INPADOC

PN - AU 74978/98 A1 19981208 [AU9874978]

TI - METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS

IN - NEVILL LELAND R

PA - MICRON TECHNOLOGY INC

AP - AU 74978/98-A 19980515 [1998AU-0074978]

PR - US 857100/97-A 19970515 [1997US-0857100]

- WO 9810226/98(US)-W 19980515 [1998WO-US10226]

IC - H01L-023/544

1/1 LEGALI - (C) LEGSTAT

PN - AU 74978/98 [AU9874978]

DT - AU-A

ACTE- 20000203 AU/MK6 [-]

APPLICATION LAPSED SECTION 142(2)(F)/REG. 8.3(3) - PCT APPLIC. NOT
ENTERING NATIONAL PHASE

UP - 2000-37

2/6 INPADOC - (C) INPADOC

PN - EP 1004142 A1 20000531 [EP1004142]

TI - METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS

LA - ENG

IN - NEVILL LELAND R [US]

PA - MICRON TECHNOLOGY INC [US]

AP - EP 98922427/98-A 19980515 [1998EP-0922427]

PR - WO 9810226/98(US)-W 19980515 [1998WO-US10226]

- US 857100/97-A 19970515 [1997US-0857100]

IC - H01L-023/544

DS - AT* BE* CH* CY* DE* DK* ES* FI* FR* GB* GR* IE* IT* LI* LU* MC* NL*
PT* SE*

1/1 LEGALI - (C) LEGSTAT

PN - EP 1004142 [EP1004142]

AP - EP 98922427/98 19980515 [1998EP-0922427]

DT - EP-P

ACTE- 19980515 EP/AE-A

EP-APPLICATION

{EP 98922427/98 19980515 [1998EP-0922427]}

- 20000531 EP/AK-A1 [+]

DESIGNATED CONTRACTING STATES IN AN APPLICATION WITH SEARCH REPORT:

AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

- 20000531 EP/A1 [+]

PUBLICATION OF APPLICATION WITH SEARCH REPORT

- 20000628 EP/17P [+]

REQUEST FOR EXAMINATION FILED

19991214

- 20010912 EP/17Q [+]

FIRST EXAMINATION REPORT

20010726

UP - 2001-37

3/6 INPADOC - (C) INPADOC

PN - JP 2001525993 T2 20011211 [JP2001525993]
AP - JP 549676/98-A 19980515 [1998JP-0549676]
PR - US 857100/97-A 19970515 [1997US-0857100]
- WO 9810226/98(US)-W 19980515 [1998WO-US10226]
IC - H01L-023/00; H01L-021/02

4/6 INPADOC - (C) INPADOC

PN - TW 392232 B 20000601 [TW-392232]
TI - METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS
IN - NEVILL LELAND R [US]
PA - MICRON TECHNOLOGY INC [US]
AP - TW 87107534/98-A 19980515 [1998TW-0107534]
PR - US 857100/97-A 19970515 [1997US-0857100]
IC - H01L-021/30

5/6 INPADOC - (C) INPADOC

PN - US 5984190 A 19991116 [US5984190]
TI - METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS
IN - NEVILL LELAND R [US]
PA - MICRON TECHNOLOGY INC [US]
AP - US 857100/97-A 19970515 [1997US-0857100]
PR - US 857100/97-A 19970515 [1997US-0857100]
IC - G06K-019/06

1/1 LEGALI - (C) LEGSTAT

PN - US 5984190 [US5984190]
AP - US 857100/97 19970515 [1997US-0857100]
DT - US-P
ACTE- 19970515 US/AE-A
APPLICATION DATA (PATENT)
{US 857100/97 19970515 [1997US-0857100]}
- 19991116 US/A
PATENT
- 20020219 US/CC
CERTIFICATE OF CORRECTION
- 20020528 US/RF
REISSUE APPLICATION FILED
20011116
UP - 2002-24

6/6 INPADOC - (C) INPADOC

PN - WO 9852226 A1 19981119 [WO9852226]
TI - METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS
LA - ENG
IN - NEVILL LELAND R
PA - MICRON TECHNOLOGY INC [US]
AP - WO US 9810226/98(US)-A 19980515 [1998WO-US10226]
PR - US 857100/97-A 19970515 [1997US-0857100]
IC - H01L-023/544
DS - AL* AM* AT* AU* BA* BB* BG* BR* BY* CA* CH* CN* CU* CZ* DE* DK* EE*
ES* FI* GB* GE* GH* GM* GW* HU* ID* IL* IS* JP* KE* KG* KP* KR* KZ*
LC* LK* LR* LS* LT* LU* LV* MD* MG* MK* MN* MW* MX* NO* NZ* PL* PT*

1/16/03

US 5,984,190

09/998594

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ZW* GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY
DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML
MR NE SN TD TG

1/2 LEGALI - (C) LEGSTAT

PN - JP 549676/98

AP - JP 549676/98 0 [1998JP-0549676]

DT - JP-A

ACTE- 19991115 JP/REFW-P

CORRESPONDS TO PCT APPLICATION

<WO 9852226> WO9852226

UP - 2002-26

2/2 LEGALI - (C) LEGSTAT

PN - WO 9852226 [WO9852226]

AP - WO 9810226/98(US) 19980515 [1998WO-US10226]

DT - WO-P

ACTE- 19980515 WO/AE-A

APPLICATION DATA

{WO 9810226/98(US) 19980515 [1998WO-US10226]}

- 19981119 WO/AK-A1 [+]

DESIGNATED STATES CITED IN A PUBLISHED APPLICATION WITH SEARCH REPORT

AL AM AT AU BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GE GH GM
GW HU ID IL IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW
MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG UZ VN YU ZW

- 19981119 WO/AL-A1 [+]

DESIGNATED COUNTRIES FOR REGIONAL PATENTS CITED IN A PUBLISHED
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GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE
DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR
NE SN TD TG

- 19981119 WO/A1 [+]

PUBLICATION OF THE INTERNATIONAL APPLICATION WITH THE INTERNATIONAL
SEARCH REPORT

- 19990225 WO/DFPE

REQUEST FOR PRELIMINARY EXAMINATION FILED PRIOR TO EXPIRATION OF 19TH
MONTH FROM PRIORITY DATE

- 19990407 WO/121

EP: THE EPO HAS BEEN INFORMED BY WIPO THAT EP WAS DESIGNATED IN THIS
APPLICATION

- 19991115 WO/ENP-A

ENTRY INTO THE NATIONAL PHASE IN:

<JP 98549676>

- 20000309 WO/REG; DE/8642 [-]

DE: IMPACT ABOLISHED FOR DE

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- 20001115 WO/NENP

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